

# INTERNATIONAL SEARCH REPORT

International Application No.

PCT/DE03/00858

## A. CLASSIFICATION OF SUBJECT MATTER

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	<p>Zusammenfassung = abstract</p> <p>Spalte = Column</p> <p>Zeile = line</p> <p>Abbildung = Figure</p>	

☐ Further documents are listed in the continuation of box C.

☐ Patent family members are listed in annex.

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Date of the actual completion of the international search

Date of mailing of the international search report

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,  
Fax: (+31-70) 340-3016

Authorized officer

## Patent Abstracts of Japan

02P05079

PUBLICATION NUMBER : 59045738  
PUBLICATION DATE : 14-03-84

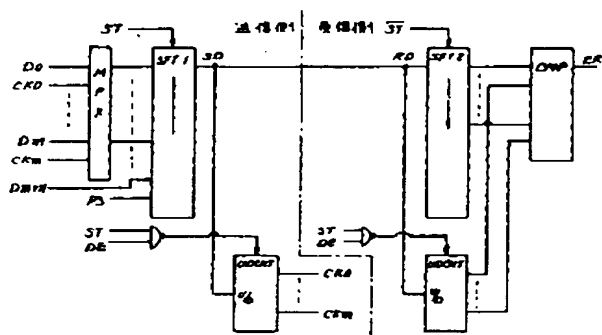
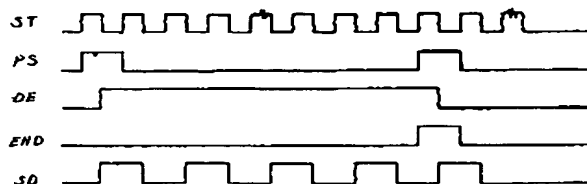
APPLICATION DATE : 07-09-82  
APPLICATION NUMBER : 57157230

APPLICANT : FUJITSU LTD;

INVENTOR : GOHARA MASAO;

INT.CL. : H04L 1/10 H03K 13/32

TITLE : SYSTEM FOR CHECKING SERIAL  
TRANSFER DATA



ABSTRACT : PURPOSE: To detect the even number of bit errors of total bits transferred to some degree with a realizing means almost the same as an LRC system.

CONSTITUTION: A data to be transmitted is set to a shift register  $SFT_1$  directly or a switching circuit MPX. The set data is shifted one by one bit and transmitted to a receiving side. A transmission signal SD is inputted to an up-down counter UDCNT to count the difference of the transmitted number of "1"s and "0"s of the transmission data. When the transmission of all data is finished, the operation of the UDCNT is stopped, a transmission end signal END is set, an MPX selects outputs  $CK_0 \sim CK_m$  of the UDCNT during the set and the result is set to the  $SFT_1$ . The set information  $CK_0 \sim CK_m$  is transmitted to the receiving side. A receiving data RD at the receiving side is inputted to an  $SFT_2$ , this is shifted and outputted as a parallel data, the RD signal is counted at the UDCNT and when the final data is received, the coincidence is checked at a comparison circuit CMP.

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